CLAIM LISTING

This listing of claims will replace all prior versions, and listings of claims in the application:

AMENDMENTS TO THE CLAIMS

1. (original) A memory array comprising:
   a. a bitline; and
   b. a plurality of memory cells, each of the plurality of memory cells having:
      i. a configuration bit terminal;
      ii. a pair of cross-coupled inverters having first and second bit nodes, wherein one of the first and second bit nodes is connected to the configuration bit terminal;
      iii. an access transistor having a first current-carrying terminal connected to the bitline, a second current-carrying terminal connected to the first bit node, and an access-transistor control terminal; and
      iv. a memory transistor having a first current-carrying terminal connected to one of the first and second bit nodes, a second current-carrying terminal connected to a power supply node, and a memory-transistor control terminal.

2. (original) The memory array of claim 1, further comprising a second configuration bit terminal connected to the first bit node, wherein the first-mentioned configuration bit terminal connects to the second bit node.

3. (original) The memory array of claim 1, further comprising a configurable resource connected to the configuration bit terminal, the configuration terminal transmitting a configuration voltage to the configurable resource.

4. (original) The memory array of claim 1, the access-transistor control terminal receiving at least one of a read control signal and a write control signal.

5. (original) The memory array of claim 1, each of the plurality of memory cells further including a programmable interconnection interposed between the first current-carrying terminal of the memory transistor and at least one of the first and second bit nodes.

6. (original) The memory array of claim 5, wherein each of the plurality of the memory cells further includes a mask-programmable interconnect providing the programmable interconnection.

7. (original) The memory array of claim 5, wherein in a first set of the plurality of memory cells the first current-carrying terminal of the memory transistor connects to the first bit node via the programmable interconnection, and wherein in a second set of the plurality of memory cells the first current-carrying terminal of the memory transistor connects to the second bit node via the programmable interconnection.

8. (original) The memory array of claim 1, each of the plurality of memory cells further including a programmable interconnection interposed between the second current-carrying terminal of the memory transistor and at least one of first and second power supply nodes.

9. (original) The memory array of claim 8, wherein each of the plurality of the memory cells further includes a mask-programmable interconnect providing the programmable interconnection.

10. (original) The memory array of claim 8, wherein in a first set of the plurality of memory cells the second current-carrying terminal of the memory transistor connects to the first power supply node via the programmable interconnection, and wherein in a second set of the plurality of memory cells the second current-carrying terminal of the memory transistor connects to the second power supply node via the programmable interconnection.

11. (original) The memory array of claim 8, wherein the first power supply node is VDD and the second power supply node is ground.

12. (original) The memory array of claim 1, wherein the cross-coupled pair of inverters is part of a static random-access memory (SRAM) cell.

13. (original) The memory array of claim 1, wherein the memory transistor is part of a read-only memory (ROM) cell.

14. (original) The memory array of claim 1, wherein the memory array is part of a configuration memory of a programmable logic device.

15. (original) The memory array of claim 1, further comprising a memory control terminal connected to the memory transistor control terminals, the memory control terminal having first and second states, wherein the first state configures the memory cells as read-only memory (ROM) and the second state configures the memory cells as random-access memory (RAM).

16. (original) The memory array of claim 15, wherein the circuit is part of a configuration memory of a programmable logic device, and wherein the first state of the memory control terminal renders the programmable logic device an application specific circuit (ASIC).

17. (original) The memory array of claim 1, wherein the power supply node is ground.

18 – 21 (canceled)

22. (original) A circuit comprising:
    a. a plurality of memory cells, each memory cell supporting a random-access memory mode and a read-only memory mode;
    b. wherein each memory cell includes a mode switch selecting one of the random-access memory mode or the read-only memory mode.

23. (original) The circuit of claim 22, further comprising an array of configurable logic resources connected to the memory cells.

24. (original) The circuit of claim 22, wherein each memory cell includes a random-access memory cell and a read-only memory cell.

25. (original) The circuit of claim 24, wherein the read-only memory cells are mask programmable.

26. (original) A programmable logic device comprising:

a. configurable logic resources having a plurality of configuration bit terminals; and

b. a plurality of memory cells, each memory cell including:

i. a configuration bit node connected to one of the plurality of configuration bit terminals of the configurable logic resources and providing a configuration-bit signal;

ii. a random-access memory element;

iii. a read-only memory element; and

iv. at least one memory control terminal selecting one of the random-access memory element and the read-only memory element to control the configuration-bit signal.

27. (original) The programmable logic device of claim 26, wherein the read-only memory element is mask programmed.

28. (original) The programmable logic device of claim 26, wherein the random-access memory element is a static random-access memory element.